This listing of claims replaces all prior versions and listings of claims in the application.

IN THE CLAIMS:

1. (currently amended) A method of forming a thermistor, comprising:

forming an isolation region in a substrate including at least an upper layer of single crystal semiconductor;

depositing a salicide precursor over said isolation region and said upper layer of single crystal semiconductor;

reacting said salicide precursor with said upper layer to form a salicide self-aligned to said upper layer, said salicide precursor not reacting to form a salicide with said isolation region; and

removing ~~an unreacted~~ a portion of said unreacted salicide precursor while preserving a portion of said unreacted salicide precursor over said isolation region as a body of said thermistor.

2. (original) The method of claim 1 further comprising:

forming a layer of interlevel dielectric (ILD) over said body of said thermistor; and

forming conductive contacts to said body of said thermistor insulated by said ILD.

3. (currently amended) The method of claim ~~2~~ 1, wherein said salicide precursor consists essentially of at least one metal selected from the group consisting of: Pt, Cu, Co, Ni, W, Ti.

4. (currently amended) The method of claim ~~2~~ 3, wherein said body of said thermistor has a thickness between 5 and 100 nm.

5. (original) The method of claim 2 wherein said interlevel dielectric includes borophosphosilicate glass (BPSG).

6. (currently amended) The method of claim ~~2~~ 3, wherein said single-crystal semiconductor consists essentially of silicon and said substrate is a silicon-on-insulator substrate having a buried oxide layer between said upper layer of single-crystal silicon and a bulk layer of single-crystal silicon.

7. (currently amended) The method of claim ~~7~~ 6, wherein said isolation region is a trench isolation region.

8. (currently amended) The method of claim ~~1~~ 3, wherein said salicide precursor is removed in a manner such that said thermistor body only overlies an isolation region.

9. (currently amended) The method of claim ~~9~~ 8, wherein said isolation region is a trench isolation region.

10. (cancelled)

11. (currently amended) The method of claim ~~1~~ 3, wherein said salicide precursor is deposited over said isolation region and said upper layer of single crystal semiconductor by sputtering.

12. (original) The method of claim 2 further comprising interconnecting first and second conductive patterns to respective ones of said contacts such that said thermistor provides local interconnection between said first and second conductive patterns.

13. (original) An integrated method of forming a thermistor, comprising:

forming an interlevel dielectric layer (ILD) above a first wiring level of an integrated circuit;

forming an embossed area in said ILD;

depositing a thermistor material in said embossed area and over said ILD;

patterning said thermistor material;

etching said ILD selective to said patterned thermistor material to define openings in said ILD above said first wiring level, said thermistor material serving as a hardmask during said etching;

forming a second wiring level in said openings;

removing said thermistor material from a surface of said ILD while permitting said thermistor material to remain in said embossed area; and

forming contacts to said thermistor material.

14. (currently amended) The method of claim ~~14~~ 13, wherein said step of forming said contacts to said remaining thermistor material includes forming a second interlevel dielectric (second ILD) above said thermistor material, forming openings in said second ILD and filling said openings with a conductor.

15. (currently amended) The method of claim ~~14~~ 13, wherein said step of forming said contacts further includes forming an insulative capping layer above said remaining thermistor material prior to forming said second ILD and extending said openings through said insulative capping layer.

16. (currently amended) The method of claim ~~14~~ 13, wherein said step of forming said second wiring level in said openings includes forming a conductive liner in said openings and thereafter depositing a conductor in said lined openings.

17. (currently amended) The method of claim ~~17~~ 16, wherein said thermistor material is selected from the group consisting of organic polymeric materials such as various anti-reflective coatings (ARCs) used in semiconductor processing, inorganic materials such as silicon oxides, silicon nitrides, silicon oxynitrides and SiC, or any metallic or semi-conducting material in an amorphous, poly-crystalline, or single-crystal form.

18. (currently amended) The method of claim ~~14~~ 13, further comprising interconnecting first and second conductive patterns to respective ones of said contacts such that said thermistor provides local interconnection between said first and second conductive patterns.

19-22. (cancelled)

23. (new) The method of claim 1, wherein said salicide precursor is reacted with said upper layer to form a salicide self-aligned to said upper layer through an annealing process.